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 Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

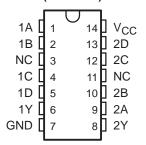
These devices contain two independent 4-input AND gates. They perform the Boolean functions $Y = A \cdot B \cdot C \cdot D$ or $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D}$ in positive logic.

The SN54F21 is characterized for operation over the full military temperature range of -55° C to 125°C. The SN74F21 is characterized for operation from 0°C to 70°C.

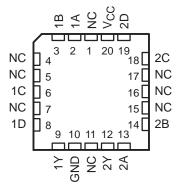
FUNCTION TABLE (each gate)

	OUTPUT			
Α	В	С	D	Υ
Н	Н	Н	Н	Н
L	Χ	Χ	Χ	L
Х	L	Χ	Χ	L
Х	Χ	L	Χ	L
Х	X	X	L	L

SN54F21 ... J PACKAGE SN74F21 ... D OR N PACKAGE (TOP VIEW)

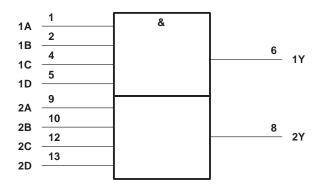


SN54F21 . . . FK PACKAGE (TOP VIEW)



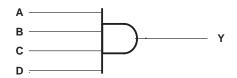
NC - No internal connection

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, J, and N packages.

logic diagram, each gate (positive logic)



TEXAS INSTRUMENTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	$-0.5\;V$ to 7 V
Input voltage range, V _I (see Note 1)	–1.2 V to 7 V
Input current range	30 mA to 5 mA
Voltage range applied to any output in the high state	-0.5 V to V_{CC}
Current into any output in the low state	40 mA
Operating free-air temperature range: SN54F21	–55°C to 125°C
SN74F21	0°C to 70°C
Storage temperature range	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54F21			SN74F21			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
VCC	Supply voltage	4.5	5	5.5	4.5	5	5.5	V	
VIH	High-level input voltage	2			2			V	
V _{IL}	Low-level input voltage			0.8			0.8	V	
liK	Input clamp current			-18			-18	mA	
lOH	High-level output current			- 1			- 1	mA	
loL	Low-level output current			20			20	mA	
TA	Operating free-air temperature	-55		125	0		70	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED		,	SN54F21				SN74F21			
PARAMETER	TES	TEST CONDITIONS			MAX	MIN	TYP [‡]	MAX	UNIT	
VIK	V _{CC} = 4.5 V,	$I_{I} = -18 \text{ mA}$			-1.2			-1.2	V	
	V _{CC} = 4.5 V,	I _{OH} = – 1 mA	2.5	3.4		2.5	3.4		V	
VOH	$V_{CC} = 4.75 \text{ V},$	I _{OH} = – 1 mA				2.7			V	
V _{OL}	V _{CC} = 4.5 V,	I _{OL} = 20 mA		0.3	0.5		0.3	0.5	V	
lį	V _{CC} = 5.5 V,	V _I = 7 V			0.1			0.1	mA	
lін	V _{CC} = 5.5 V,	V _I = 2.7 V			20			20	μΑ	
IIL	$V_{CC} = 5.5 \text{ V},$	V _I = 0.5 V			- 0.6			- 0.6	mA	
los§	V _{CC} = 5.5 V,	VO = 0	-60		-150	-60		-150	mA	
Іссн	V _{CC} = 5.5 V,	V _I = 4.5 V		2.8	4.3		2.8	4.3	mA	
ICCL	V _{CC} = 5.5 V,	V _I = 0		4.7	7.3		4.7	7.3	mA	

[‡] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

[§] Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

SN54F21, SN74F21 DUAL 4-INPUT POSITIVE-AND GATES

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switching characteristics (see Note 2)

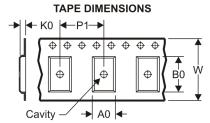
PARAMETER	FROM (INPUT)	TO (OUTPUT)	UTPUT) $T_A = 25^{\circ}C$			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω , T_A = MIN to MAX †				UNIT	
			MIN	′F21 TYP	MAX	SN54 MIN	IF21 MAX	SN74 MIN	F21 MAX		
			4			4		4			
t _{PLH}	A, B, C, or D	~		1	3.2	4.7	1	5.6	1	5.3	ns
^t PHL	А, В, О, ОГВ	1	1.5	3.4	5.1	1.5	5.9	1.5	5.5	110	

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions. NOTE 2: Load circuits and waveforms are shown in Section 1.



TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74F21DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1





*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74F21DR	SOIC	D	14	2500	346.0	346.0	33.0

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